ABSTRACT

An analog video bus architecture that utilizes the column parallel nature of CMOS imagers and more specifically Active Column Sensors, that eliminates the need for multi-port imagers, by increasing the useable bandwidth of single port imagers. An adaptation of this invention allows for either binning or interpolation of pixel information for increased or decreased resolution along the columns and more specifically for ACS imagers binning or interpolation along the rows. In this bus, the single video bus is replaced by multiple video buses and instead of selecting only one column for reading multiple columns are also pre-selected in-order to pre-charge the video bus. The video buses are then de-multiplexed back on to one port at the desired element rate. This architecture utilizes the column oriented video bus of CMOS imagers. It divides the large video bus capacitance by the number of video buses used. In addition, it allows multiple pixel time constants to precharge the video bus. The best commercially available imager designs now claim 40 MHz per analog port and suffer from reduced signal to noise ratios. To overcome this fundamental bandwidth limitation, imager designs in the past have had to increase the number of video ports per imager to achieve high frame rates. Multiple ports per imager breaks the focal plane into segments that are typically reassembled via post processing in a host computer. The other problem with multiple ports is each segment of the imager will have its own offsets and resultant Fixed Pattern Noise (FPN). PVS-Bus™ eliminates the objectionable segmentation and simplifies high-speed system design. Also, by utilizing the column parallel nature of CMOS video buses a method and improved method of using the PVS-Bus of binning and interpolation is described which results in increased frame rate, and for decreased or increased resolution.